Implementation of LFSR Reseeding Technique in NLFSR Based Test Pattern on FPGA

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Abstract— This project describes a Pseudorandom test pattern generator (PRPG) with Non-Linear Feedback shift register (NLFSR) .It is mainly suited for Built in self Test (BIST) circuits in order to achieve low power. The LFSR Reseeding techniques is implemented along with NLFSR to generate new test patterns and it is used to drive the Phase shifters then it produces the binary sequences with pre-selected toggling activities(PRESTO).This technique is further preferred to achieve desired fault coverage and low power. The Proposed scheme is used to reduce the overall area of the architecture and it is used for industrial designs which are reported in experimental results.

Index Terms — BIST [Built in self test], PRPG [pseudorandom pattern generator], NLFSR [Non-linear feedback shift register],PRESTO[pre-selected toggling activities].

1. INTRODUCTION

Built in self test is a design methodology in which part of the circuit is used to test itself and it is widely used as a better solution for intellectual property core in system on chip(SOC) design[1].NLFSR is used to generate the pseudorandom test patterns and it is used to drive the phase shifter of the PRESTO Generator and it is applied to the circuit under test(CUT). The NLFSR is used to generate pseudorandom sequences and it is used for various applications such as data compression error detection and correction, Testing and cryptography. As the size and complexity of systems-on-chips increases, the power dissipation during testing becomes very important problem. During scan shifting, more transitions occur in the flip-flops compared to normal functional operation[4]. This problem is further pseudorandom filling of the unassigned input values is employed. Excessive power dissipation during test can increase manufacturing costs by requiring the use of a more expensive chip packaging or causing unnecessary yield loss.

The methods used in BIST methods are Checker board method, marching test, pseudorandom number generator. Built-In Self-Test is a self testing mechanism. That can be used to check the functionality of the device[9]. It has been shown to be an effective design for testability technique in which some on-chip test structure is used to test the digital circuit itself. Pseudo-random testing based on linear feedback shift registers is widely used because of its simplicity and effectiveness.

2. METHODOLOGY

a. NLFSR

Non-linear feedback shift registers [NLFSR] are a generalization of linear feedback shift register [LFSR] in which the current state is a non-linear function of the previous state. In the Galois configuration the feedback can be applied to every bit and it decreases the propagation time and increasing the throughput. The feedback shift register is a type of digital oscillator[3]. There are numerous applications of NLFSR such as code generation, counting and sequence recognition (or) decoding. In recent years, nonlinear feedback shift registers have received much attention in designing many cryptographic primitives such as pseudorandom sequence generators (PRSGs), stream ciphers, and lightweight block ciphers to provide security in communication systems.

Galois NLFSRs do not concatenate every tap to produce the new input (the XOR operation is done within the NLFSR and XOR gates are run in parallel, therefore the propagation times are reduced to that of one XOR rather than a whole chain), thus it is possible for each tap to be computed in parallel, increasing the speed of execution. Nonlinear feedback shift registers (NLFSRs) are used to construct pseudorandom generators for stream ciphers.

b. BLOCK DIAGRAM OF PRESTO GENERATOR

The PRPG is connected with the Phase shifter to produce the pseudorandom sequences. The PRPG can be implemented with NLFSR. The n-hold latches are placed in front of the phase shifter and the toggle control registers are used to control each latches[7]. If the inputs are enabled means the data are going from PRPG to the Phase shifter then it is said to be in Toggle mode. When the latch is disabled the captured bits are stored for a number of clock cycles and the constant data are injected to the phase shifter. Now it acts as in hold

mode. The scan chains are in hold mode because the phase shifter output is produced by using the latches.

The Toggle control registers supervises the latches. If the values are between 0's or 1's.Wher 1 indicates the latches in the Toggle mode and 0's indicates the latches are in the Hold mode. The enable inputs are given to the shift register are produced in probabilistic fashion by using the PRPG with a programmable set of weights. Pseudorandom test patterns are random in nature and it replaces original random sequences. Pseudorandom test pattern generation is a simplest method of creating tests. It uses pseudorandom number generator to generate test vectors and relies on logic simulation to compute good machine results and fault simulation to calculate the fault coverage of the generated vectors. The four AND gates determines the weights producing 1's with a probability of 0.5, 0.25, 0.125 and 0.0625 respectively. The probabilities are chosen beyond the simple powers of 2 by using the OR gates. The user defined switching activity can be obtained by using a 4-Bit register. For example, the switching code 0100 is set to 1 means on an average of 25% of the latches 25% of the control register stages are enabled. The four input NOR gate detects the switching code 0000 and it is used to switch the Low power (LP) functionality off. The Phase shifter output is given to the Circuit Under Test(CUT).In weighted pseudorandom test pattern generator,the distribution of 0s and1s produced on the output lines is not uniform.The different parts of a circuit may be tested more effectively than other parts by pseudorandom patterns having different distriutions.Once the weight of the signals are determined,the appropriate circuit can be designed to generate pseudorandom having the desired distributions. In weighted pseudorandom test pattern generator,the distribution of 0s and1s .

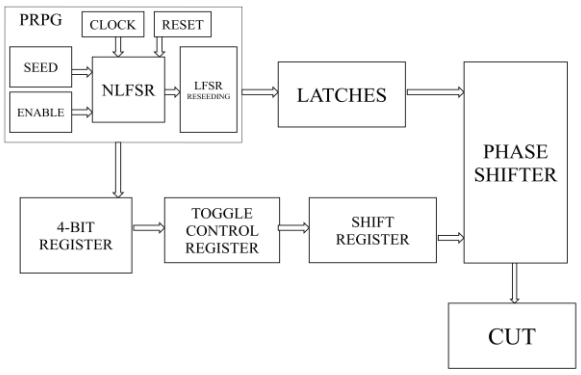

Fig 1.Block diagram of PRESTO Generator

3. LFSR RESEEDING TECHNIQUE

The basic idea in LFSR reseeding is to generate deterministic test cubes by expanding seeds. A seed is an initial state of the LFSR that is expanded by running the LFSR. Given a deterministic test cube, a corresponding seed can be computed by solving a set of linear equations (one equation for each specified bit) based on the feedback polynomial of the LFSR[8]. Since typically only 1%-5% of the bits in a test vector are specified, most bits in a test cube do not need to be considered when a Seed is computed because they are don't care bits.

Therefore, the size of a seed is much smaller than the size of a test vector. Consequently, reseeding can significantly reduce test-data storage and bandwidth. Several reseeding schemes have been proposed to reduce test storage. The most important parameters that are considered when evaluating the quality of test pattern compression are: keeping 100% test coverage, number of test clock cycles (test length), number of tester channels devoted to the CUT test, hardware overhead, possibility of non-valid responses masking, energy spent on testing (low test energy, constrained test power).

LFSR reseeding scheme to significantly reduce power consumption during test (preliminary results were presented in [3]). LFSR reseeding is a good solution for testing large SOC, but causes excessive power dissipation. This paper has proposed a new low power scheme using the LFSR reseeding. The proposed scheme divides each test cube into several non-transitional or transitional blocks, and can eliminate the transitions introduced in the non-transitional blocks. The original test cube is encoded into the low power test cube. The proposed encoding scheme provides a way to reduce the test power for LFSR. And also improving the test compression is achieved.

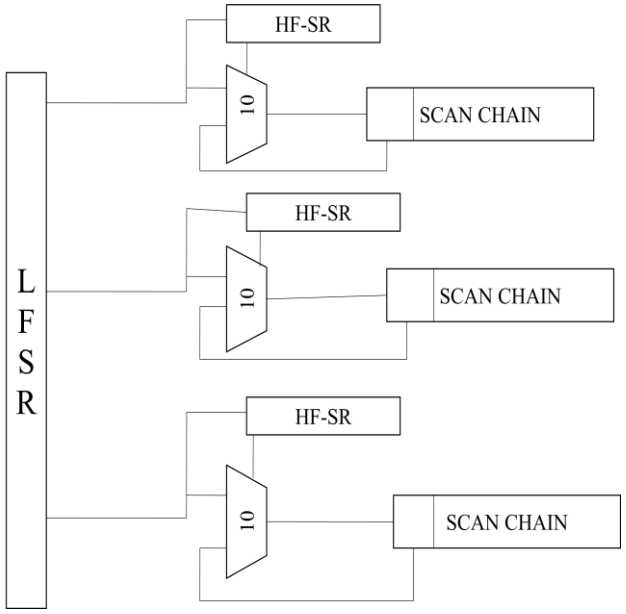

Fig 2.LFSR Reseeding techniques

The LFSR Reseeding technique based PRESTO generator architecture is shown in fig3The test patterns are split up into two intervals namely toggle and hold periods. To move the generator back and forth between these two states, a T-type flip-flop is used here and it switches whenever there is a 1 on its data input. If it is set to 0, the generator enters the hold period with all latches temporarily disabled regardless of the control register content. This is accomplished by placing AND gates on the control register outputs to allow freezing of all phase shifter inputs[6][7].

The property can be used in SOC designs where only a single scan chain crosses a given core, and its abnormal toggling may cause locally unacceptable heat dissipation that can only be reduced due to temporary hold periods to the scan chains. Two additional parameters kept in 4-bit Hold and Toggle registers determine how long the entire generator remains either in the hold mode or in the toggle mode, respectively[2]. To terminate either mode, a 1 must occur on the T flip-flop input. This weighted pseudorandom signal is produced in a manner similar to that of weighted logic used to feed the shift register. The T flip-flop controls also four 2-input multiplexers routing data from the Toggle and Hold registers. It allows selecting a source of control data that will be used in the next cycle to possibly change the operational mode of the generator.

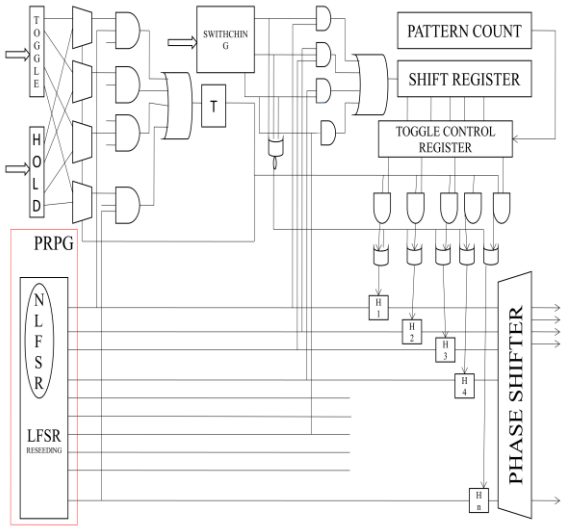

Fig.3 Architecture of PRESTO Generator

For example, when in the toggle mode, the input multiplexers observe the Toggle register. Once the weighted logic outputs 1, the flip-flop toggles, and as a result all hold latches freeze in the last recorded state. They will remain in this state until another 1 occurs on the weighted logic output A scan switching profile when deploying the PRESTO generator in a hypothetical environment with 15 scans chains.

Test patterns are divided into hold and toggle intervals of random length, while LP scan chains remain still for the entire duration of a single test pattern. When using the PRESTO generator with an existing DFT flow, all LP registers are either loaded once per test or every test pattern. The registers loaded only once act as test data registers or are parts of an IJTAG network, and are initialized by the test setup procedure. They are triggered using a slow scan shift clock and operate at a very low speed thereby imposing no timing constraints. Although the remaining registers are loaded once per test pattern (also at the scan shift speed), timing is not compromised because of shallow logic generating bits to be loaded serially into the registers[1]. With the help of shadow registers, values remain unchanged during capture.

a. Clock gating techniques

Clock gating is a technique that enables the saving of electrical power used by computer processors. It ensues power saving by turning on a functional block clock, but only when required. it is popularly used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit Pruning the clock disables portions of the circuitry so that the flip-flops in them do not to switch states. Switching states consumes more power. when not being switched, the switching power consumption goes to zero, and only leakage currents are incurred[4].

Clock gating works by taking the enable conditions attached to registers and use them to gate the clocks ,Therefore it must be imperative that a design contain these enable conditions in order to use and benefit from clock gating.This clock gating technique can also save significant die area as well as power it removes large number of muxex and replaces them with clock gating logic.

4. SIMULATION RESULTS

The approach is validated by experiments on five varietyof scan architecture and it is used in five industrial designswith 128-bit NLFSR implementing a primitive polynomialx^128+x^65+x^33+x^25+x^16+x^8+1 and LFSR Reseeding techniques ae used to eliminate the old test patterns and generate the new test patterns and it feeding the phase shifter with 10,000 test patterns..

a. Random test patterns

The NLFSR generate more number of random test patterns with the help of LFSR Reseeding techniques. The Patterns are generally fault simulated and detected faults are withdrawal from the list and it takes less amount of power and area. the test patterns are produced with improved fault coverage. The phase shifters are synthesized separately and then the switching activity is compared with the resultant toggling rates to achieve better performance. The test bench waveform

is shown in fig:6,the PRESTO generator and the combined NLFSR and LFSR Reseeding techniques based pseudorandom test pattern are integrated in the design power dissipations are reduced due to the weighted logic used to determine the weights of random signals

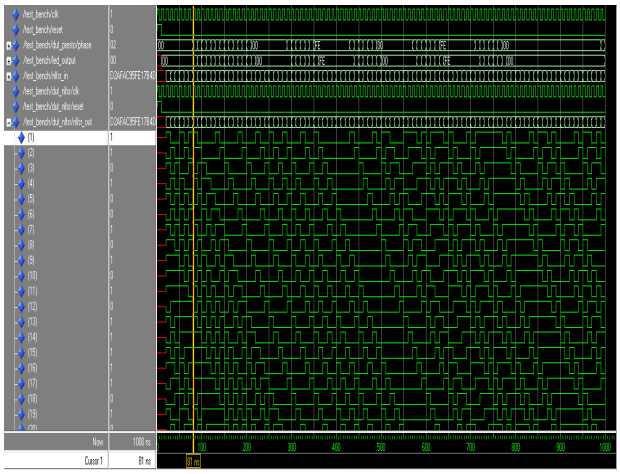

Fig.4 Random test patterns

The stuck at fault coverage increases with the increased switching activity. The switching activity is determined for each and every test pattern. The phase shifters are synthesized separately and then the switching activity is compared with the resultant toggling rates to achieve better performance.

b. Testbench waveform

The test bench waveform is shown in fig:6,the PRESTO generator and the combined NLFSR and LFSR Reseeding techniques based pseudorandom test pattern are integrated in the design .The latches are designed in such a way that it acts either in hold or toggle mode. The phase shifter output is produced by combining the three hold period values and it consumes low power for the operations. The power dissipations are reduced due to the weighted logic used to determine the weights of random signals. The test patterns produced by the PRPG are transformed in a more deterministic manner. The toggle control registers are driven by the test data and the test patterns are produced with improved fault coverage[3]. The phase shifters are synthesized separately and then the switching activity is compared with the resultant toggling rates to achieve better performance. The phase shifter output is produced by combining the three hold period values and it consumes low power for the operations. The test bench waveform is shown in fig:6,the PRESTO generator and the combined NLFSR and LFSR Reseeding techniques The latches are designed in such a way that it acts either in hold or toggle mode

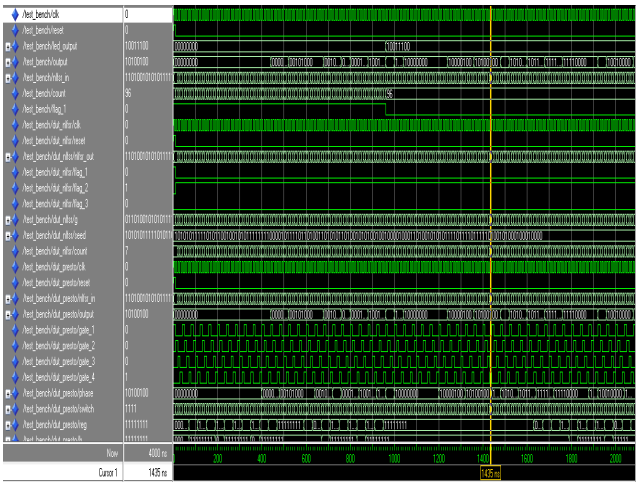

Fig.5 Testbench waveform

C.Synthesis report

The clock gating technique reduces the power dissipations and the number of slices used for the operation is reduced more than 25% compared to the previous work. The test patterns produced by the PRPG are transformed in a more deterministic manner. The higher fault coverage can be obtained with shorter test time. In general power dissipation of a system is higher in test mode than the normal mode. In scan mode each flip-flops can be converted into a scan register by adding one extra multiplexer. In normal mode the flip-flops act as a normal memory elements. The extra power can cause problems such as instantaneous power that cause circuit damage, formation of hot spots, difficulty in performance verification and reduction of system lifetime and product yield.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	136	4656	2%
Number of Slice Flip Flops	186	9312	1%
Number of 4 input LUTs	228	9312	2%
Number of bonded IOBs	10	232	4%
Number of GCLKs	1	24	4%

Fig.6 Synthesis report

To improve the fault detection probabilities, the distribution of number of 1s in the toggle control register are to be determined. The number of scan chains, phase shifter, switching code, hold and toggle values are calculated automatically by using the size of PRPG. The test patterns are

produced with desired toggling levels and the scan chains also balanced.

5. CONCLUSION

In this paper low power pseudorandom test pattern generator is designed with NLFSR and LFSR reseeding techniques.NLFSR is ued to generate pseudorandom patterns with peselected toggling activities by using Galois field method.LFSR Reseeding techniques are used to eliminate the old test patterns and generate the new test patterns to detect the faults in the circuit.Further clock gting techniques are used to achieve low power with reduced area.

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